What is claimed is:

1. In an electronic system including a plurality of components, a system for frequency margin testing of one or more of said components, comprising:

a controller internal to said electronic system; and

a digital frequency synthesizer in communication with said controller and with one or more of said components, said frequency synthesizer generating one or more test frequencies for application to said one or more components in response to commands from said controller.

2. The margin testing system of claim 1, further comprising:

a diagnostics software executing to collect and analyze data regarding a response of selected components of said system to said test frequencies.

3. The margin testing system of claim 2, wherein said controller executes the diagnostics software.

4. The margin testing system of claim 1, further comprising:

a hardware monitor in communication with said controller and said frequency synthesizer to measure values of said one or more test frequencies and to transmit said measured values to said controller.

5. The margin testing system of claim 4, wherein said hardware monitor communicates with selected ones of said components to receive data regarding response of said components to said one or more test frequencies.

6. The margin testing system of claim 1, wherein said controller transmits command signals to said frequency synthesizer to cause the synthesizer to generate said one or more test frequencies.

7. The margin testing system of claim 1, wherein said controller is a Baseboard Management Controller (BMC).

8. The margin testing system of claim 7, wherein said BMC implements Intelligent Platform Management Interface (IPMI) protocol.

9. The margin testing system of claim 7, further comprising:

an I^2C-based bus for providing communication between said BMC and said frequency synthesizer.

10. The margin testing system of claim 9, wherein said I^2C-based bus comprises:

an IPMB bus.

11. The margin testing system of claim 1, wherein said frequency synthesizer receives an input reference clock signal, and in response to a command signal from said controller, generates an output clock signal as a multiple of said reference clock signal.

12. The margin testing system of claim 11, wherein said frequency synthesizer applies said output clock signal as a test frequency to said one or more components for frequency margin testing thereof.

13. The margin testing system of claim 1, wherein said frequency synthesizer generates each one of a plurality of test frequencies based on a pattern of input bits received from the controller.

14. The margin testing system of claim 1, wherein said controller initiates margin testing in response to commands from an external system.

15. The margin testing system of claim 14, wherein said external system comprises:

a console in communication with said controller via a serial bus.

16. The margin testing system of claim 14, wherein said external system comprises:

a remote computer in communication with said controller.

17. The margin testing system of claim 16, wherein said remote computer communicates with said controller via a network-based connection.

18. The margin testing system of claim 14, wherein said external system includes a scripting entity for generating commands for transmission to said controller.

19. The margin testing system of claim 1, wherein said one or more components receive nominal clock frequencies in the absence of said test frequencies.

20. A computer system, comprising:

a processor;

a plurality of components in communication with said processor for performing a plurality of tasks;

a controller; and

a digital frequency synthesizer in communication with said controller and one or more of said components, said synthesizer generating one or more test frequencies for application to selected ones of said one or more components for frequency margin testing thereof in response to commands from said controller.

21. The computer system claim 20, wherein said controller comprises:

a BMC.

22. The computer system of claim 21, wherein said BMC implements an IPMI protocol.

23. The computer system of claim 20, further comprising:

an I^2C-based bus for providing communication between said BMC and said frequency synthesizer.

24. The computer system of claim 20, wherein said computer system is a server.

25. A method for frequency margin testing of one or more components of a computer system, having an internal controller and a digital frequency synthesizer, in communication with said internal control, for applying clock frequency to said components, comprising:

causing the controller to transmit one or more commands to said synthesizer to cause the synthesizer to generate one or more test frequencies for application to said components; and

monitoring response of said computer system to each of said test frequencies.

26. The method of claim 25, further comprising:

executing a diagnostics software to obtain response of the system to each of said test frequencies.

27. The method of claim 25, further comprising:

selecting said controller to be a BMC implementing an IPMI protocol.

28. The method of claim 27, further comprising:

employing an I^2C-based bus to provide communication between said BMC and said frequency synthesizer.

29. The method of claim 25, wherein the step of causing the controller to transmit commands to the synthesizer comprises:

transmitting a bit pattern from said controller to said frequency synthesizer to set an output of said synthesizer to a selected value based on said bit pattern.